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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,153	08/27/2004	ChangSheng Ying	21736-000200	5152

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,153	YING, CHANGSHENG	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This application 10/605,683 has been examined. Claims 1-16 are pending.

Claim Objections

1. Claims 1 and 15 are objected to because of the following informalities: With respect to claims 1 and 15, the preamble should state the intended use or purpose of the invention. C.R. Bard v. M3 Systems, Inc. 157 F.3d 1340, 48, 48 USPQ2d 1225,1230-31 (Fed. Cir. 1998). Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-9 and 11-16 are rejected under 35 U.S.C. 102(e)** as being anticipated by Chang et al. (6,470,489).

4. With respect to claims 1 and 15, Chang teaches a method comprising: providing a first layout database of an IC design, wherein the first layout database is obtained before OPC treatment (Figure 8, #810, i.e. design database before any corrections); providing a second layout database of the IC design, wherein the second database is

obtained after OPC treatment (Figure 8, #860, i.e. design database after OPC correction); finding a location of a first structure in the first layout database (Col 21, lines 5-18, i.e. checking and flagging areas/locations from the ideal layout –ideal layout is before OPC correction which is the first layout database); finding the first structure in the second layout database based on its location in the first layout database (Col 21, lines 5-18, i.e. flagging areas in the corrected design [second database] and using that areas location from the ideal layout [first database]); simulating a resulting layout output for the first structure using the second layout database (Col 21, lines 5-18, i.e. the resulting corrected [second database] mask's simulated image is converted into polygons –where all first polygons [and/or structures, areas, geometries] are simulated for the entire IC); measuring a first critical dimension of the first structure from the resulting layout output for the first structure (Figure 21, #2120, i.e. edge deviation [edge critical dimension] of a particular geometry [structure] between layout output and ideal layout); comparing the first critical dimension of the first structure to a drawn dimension of the first structure from the first database (Col 20, lines 38-63, i.e. corrected layout's image is compared to ideal layout [first database] itself); and flagging the first structure in the first or second database if the first critical dimension is less than the first drawn dimension in the first database (Col 21, lines 5-18, i.e. flagging areas [from the corrected data's layout image, i.e. second database] that do not conform to ideal image [first database]).

5. With respect to claim 2, Chang teaches all the elements of claim 1, from which the claim depends, as described above. Chang teaches the method of claim 1, wherein the step of flagging the first structure in claim 1 (see above) is replaced by flagging the

first structure in the second database if the first dimension is less than the first drawn dimension plus a tolerance value in the first database (Col 21, lines 5-19, i.e. checking and flagging locations [from corrected image, i.e. second layout] that are not within the prescribed bounds [i.e. tolerances on a specific dimension]).

6. With respect to claim 3, Chang teaches all the elements of claim 2, from which the claim depends, as described above. Chang teaches the method of claim 2, wherein the tolerance value is specified by the user (Figure 21, #2120, i.e. Tolerance is indicated as an input to block 2120, which implies a user specification, because Chang does not indicate that any other block/process provides this tolerance input-value, see also Col 20, lines 39-55).

7. With respect to claim 4, Chang teaches all the elements of claim 1, from which the claim depends, as described above. Chang teaches the method of claim 1, wherein the first and second layout databases are in GDS-II format (Col 5, lines 18-23, i.e. ideal layout [first database] is in GDS-II; Col 4, lines 55-60, i.e. corrected layout [second database] is in GDS-II format).

8. With respect to claim 5, Chang teaches all the elements of claim 1, from which the claim depends, as described above. Chang teaches the method of claim 1 wherein the selected structure is at least one of a transistor gate, transistor end-cap, line, line-end, via and gap, or contact and gap (Col 14, lines 30-60, i.e. patterns involving transistor gates and line-end shortening).

9. With respect to claim 6, Chang teaches all the elements of claim 1, from which the claim depends, as described above. Chang teaches the method of claim 1 wherein

the step of finding a location of a first structure in the first layout database is performed using pattern recognition (Col 4 line48 – Col 5 line 5, i.e. edge-checking technique that generates the geometry of the printed patterns in a GDS-II format, said format is processed by a design-rule checker which determines locations of areas/patterns with design errors, and the ideal layout [first database] contains said areas/patterns).

10. With respect to claim 7 and 8, Chang teaches all the elements of claim 1, from which the claims depend, as described above. Chang teaches the method of claim 1, wherein when the first structure is a transistor gate and the first critical dimension is gate length or gate width (Col 14, lines 31-68, i.e. discussion of transistor gates and their OPC correction issues).

11. With respect to claim 9, Chang teaches all the elements of claim 1, from which the claim depends, as described above. Chang teaches the method of claim 1, further comprising: building a model of a process, to be used to fabricate the integrated circuit design, and wherein the step of simulating a resulting layout output for the first structure using the second layout database is performed using this model of the process (Figure 21, #2210, i.e. Simulate corrected layout's geometry [second layout database] for all geometries).

12. With respect to claim 11, Chang teaches a method executing in a computer-aided design system for designing circuitry prior to physical implementation (Col 1, lines 55-60, i.e. CAD tool to design/translate circuit into completed IC), wherein the method checks compliance of a simulated layout output (Col 4, lines 1-10, i.e. design rule checking of a OPC corrected design that is simulated) of a selected structure (Col 21,

lines 1-5, i.e. polygon(s) of the OPC-corrected design) provided in a first database of an integrated circuit design after optical proximity correction treatment (Figure 12, #1210, i.e. OPC-corrected design data; also Figure 2, #260) to a drawn dimension of the selected structure provided in a second database of the integrated circuit design before optical proximity correction treatment (Col 20, lines 5-20, i.e. geometry dimension of ideal layout – from data prior to OPC correction), the method comprising: providing a design rule that is violated when a measured critical dimension of the simulated layout output for the selected structure is less than the drawn dimension of the selected structure (Col 21, lines 1-18, i.e. a flag [violation] occurs when areas [dimensions] of the simulated design do not conform to the ideal image's design-rule checking requirements –violation occurs because dimensions may be less/greater, or outside particular boundaries); applying the design rule to at least a portion of the integrated circuit design (Col 21, lines 1-18, i.e. repeatedly checking and flagging locations that are not within prescribed bounds [design rule]); and providing a user-discernable indication of any violation of the design rule (Col 18, lines 3-9, i.e. a re-design decision must be made by user after notification that design rules have not been met).

13. With respect to claim 12, Chang teaches all the elements of claim 11, from which the claim depends, as described above. Chang teaches the method of claim 11 wherein the selected structure is at least one of a transistor gate, transistor end-cap, line, line-end, via and gap, or contact and gap (Col 14, lines 30-60, i.e. patterns involving transistor gates and line-end shortening).

14. With respect to claim 13, Chang teaches all the elements of claim 11, from which the claim depends, as described above. Chang teaches the method of claim 11, wherein the step of providing a design rule that is violated when a measured critical dimension of the simulated layout output for the selected structure is less than the drawn dimension of the selected structure is replaced by the step of providing a design rule that is violated when a measured critical dimension of the simulated layout output for the selected structure is less than the drawn dimension of the selected structure plus a tolerance value (Col 21, lines 1-25, i.e. discussion of prescribed bounds and satisfactory tolerance criteria).

15. With respect to claim 14, Chang teaches all the elements of claim 13, from which the claim depends, as described above. Chang teaches the method of claim 13, wherein the tolerance value is specified by the user (Figure 21, #2120, i.e. Tolerance is indicated as an input to block 2120, which implies a user specification, because Chang does not indicate that any other block/process provides this tolerance input-value, see also Col 20, lines 39-55).

16. With respect to claim 16, Chang teaches all the elements of claim 15, from which the claim depends, as described above. Chang teaches the method of claim 15 further comprising: flagging the first structure in the second database if the first critical dimension is less than the first drawn dimension in the first database (Col 21, lines 5-18, i.e. flagging areas [from the corrected data's layout image, i.e. second database] that do not conform to ideal image [first database]).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. **Claim 10 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Chang et al. (6,470,489) in view of Garza et al. (6,269,472).

19. With respect to claim 10, Chang teaches all the elements of claim 1, from which the claim depends, as described above. Chang fails to teach consulting a look-up table. However, Garza teaches storing a series of discrete points corresponding to OPC correction values into a look-up table which can then be used to simulate a corrected layout (Col 10, lines 30-43). Note that Chang uses the aid of correction values to produce a layout (see Chang, Figure 2, i.e. correction data 260 used in final data layout 275). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Garza into the method/system of Chang because Garza states that a look-up table generally simplifies software operations and speeds up computation, and such software operations and computation are necessary in simulating a layout.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suchin Parihar
Examiner
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800